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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,107	03/31/2004	Joseph C. Coffey	2316.1834US01	5190

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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	PAPER NUMBER
2841	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,107	COFFEY ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/18/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/18/2006 has been entered.

Response to Amendment

2. Amendment filed on 10/13/2006 has been entered.
In response to the Office Action dated 08/09/ 2006, Applicants have amended claims 1 and 8.
Claims 1-13 are now pending in the application.

Response to Arguments

3. Applicant's arguments filed 10/13/2006 and 12/18/2006 have been considered but are moot in view of the new grounds of rejection. Nevertheless, the Examiner points out, in response to applicant's arguments that Jennison's reference teaches away. Jennison teaches to use punch down connector to create a card edge socket with permanently connected contact pairs which can be easily disconnected and re-routed multiple phone lines (column 1, lines 39-59), which is the similar to subject matter of the application – using the interconnect location to selectively access to the termination locations (Specification, page 2, lines 1-3).

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees.

A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal

disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4.1. Claims 1-7 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of copending Application No. 10/871698. Although the conflicting claims are not identical, they are not patentably distinct from each other.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4.2. With respect to claims 1 and 8 claim 1 and 10 of Application No. 10/871698 teaches all of the limitations exactly except:
1. claims 1 and 8 disclose : "mounted to the front major surface of the back plane" and only "mounted to the back plane " in claims 1 and 10 of Application No. 10/871698, respectively. However this limitations in claims 1 and 10 of Application No. 10/871698 still reads on claims 1 and 8 of application.

4.3. Claim 1 correspond to claim 1 of Application No. 10/871698. Claim 2 correspond to claim 2 of Application No. 10/871698. Claim 3 correspond to claim 3 of Application No. 10/871698. Claim 4 correspond to claim 4 of Application No. 10/871698. Claim 5 correspond to claim 5 of Application No. 10/871698. Claim 6 correspond to claim 6 of Application No. 10/871698. Claim 7 correspond to claim 7 of Application No. 10/871698. Claim 8 correspond to claim 10 of Application No. 10/871698. Claim 9 correspond to claim 11 of Application No. 10/871698. Claim 10 correspond to claim 12 of Application No. 10/871698. Claim 11 correspond to claim 13 of Application No. 10/871698 Claim 12 correspond to claim 14 of Application No. 10/871698. Claim 13 correspond to claim 15 of Application No. 10/871698.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5.1. Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennison (Patent #6535602) hereinafter Jennison, and in view of Gerke et al. (Patent # 6068503) hereinafter Gerke.

As to claim 1: Jennison discloses in Fig. 1 and 2 a patch panel comprising: a back plane 1 having a front major surface and, a back major surface facing in an opposite direction; a plurality of pairs of termination locations 4 and 2 mounted to the back plane 1, each termination location including a patch cord access device (for instance, telephone jack) defining electrical contacts connected to the back plane for electrically connecting to conductors in a patch cord; a plurality of interconnect locations 3 mounted to the back plane, each interconnect location defining a card edge socket with normally connected contact pairs connected to the back plane; circuitry on the back plane 1 for connecting each termination location 4 and 2 of each pair to one of the interconnect locations (column 3, lines 24-31).

except Jennison does not teach each contact pair electrically connected in the absence of an interconnect module introduced into the card edge socket.

Gerke discloses in Fig. 5 and 6 contact pair 25, 27 electrically connected in the absence of an interconnect module 15 introduced into the card edge socket.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Jennison to include in his invention each contact pair electrically connected in the absence of an interconnect module introduced into the card

edge socket in order to allow the strip to be wired up conveniently and reliably, as well as in visually clear manner, as taught by Gerke (column 2, lines 23-26)

As to claim 2: Jennison, as modified, discloses the patch panel as applied claim 1 above, wherein one of the pairs of termination locations includes two RJ45 jacks (column 2, lines 12-17 and column 3, lines 31-35) .

5.2. Claims 5- 9, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennison and in view of Gerke, and further in view of Carlson et al. (Patent # RE37125) hereinafter Carlson.

As to claim 8: Jennison discloses in Fig. 1 and 2 a patch panel comprising: a back plane 1 having a front major surface and a back major surface; a plurality of pairs of termination locations 4 and 2 mounted to the front major surface of the back plane 1, each termination location including a patch cord access device defining electrical contacts connected to the back plane for electrically connecting to conductors in a patch cord; a plurality of interconnect locations 3 for each receiving a removable circuit module, each interconnect locations mounted to the front major surface of the back plane and including normally connected contact pair [Jannison teaches to use jumpers 3, Fig. 1 with punch down connector to create a card edge socket with permanently connected contact pairs 4 which can be easily disconnected and re-routed multiple phone lines (column 1, lines 39-59); circuitry on the back plane 1 for connecting each termination location 4 and 2 of each pair to one of the interconnect locations],

except Jennison does not teach each contact pair of a plurality of interconnect locations electrically connected in the absence of a circuit module;

Gerke discloses in Fig. 5 and 6 contact pair 25, 27 electrically connected in the absence of an interconnect module 15 introduced into the card edge socket.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Jennison to include in his invention that each contact pair

electrically connected in the absence of a circuit module in order to allow the strip to be wired up conveniently and reliably, as well as in visually clear manner, as taught by Gerke (column 2, lines 23-26)

Jennison also doesn't teach at least one removable circuit module mounted to one of the interconnect locations, the removable circuit module including circuitry connected to interconnect location for connecting to one of the pairs of termination locations.

Carlson discloses in Fig. 1 at least one removable circuit module 22 mounted to one of the interconnect locations 20, the removable circuit module including circuitry connected to interconnect location 20 for connecting to one of the pairs of termination locations 30 32 (column 5, lines 18-28).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that at least one removable circuit module mounted to one of the interconnect locations, the removable circuit module including circuitry connected to interconnect location for connecting to one of the pairs of termination locations, as taught by Carlson because Carlson teaches that such a configuration would provide an interface between a utility distribution network and subscriber owned equipment (column 2, lines 22-26).

As to claim 9: Jennison discloses the patch panel having all of the claimed features as discussed above with respect claim 8, wherein one of the pairs of termination locations includes two RJ45 jacks column 2, lines 12-17 and column 3, lines 31-35).

As to claim 5: Jannison discloses the patch panel having all of the claimed features as discussed above with respect claim 1,

except , Jennison doesn't explicitly teach the patch panel comprising a module defining an edge contact sized for receipt in one of the card edge sockets, of one of the interconnect locations.

Carlson discloses in Fig. 1 the patch panel 16 comprising a module 22 defining an edge contact sized for receipt in one of the card edge sockets 20, of one of the interconnect locations (column 4, lines 18-29).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that the patch panel comprising a module defining an edge contact sized for receipt in one of the card edge sockets, of one of the interconnect locations as taught by Carlson because Carlson teaches that such connectors is adapted to receive a complementarily shaped end portion of a service module.

As to claims 6 and 12: Jennison discloses the patch panel having all of the claimed features as discussed above with respect claim 1(8),

except , Jennison doesn't explicitly teach a power module mounted to the major surface of the back plane 16 and electrically connected to the circuitry.

Carlson discloses in Fig. 1 a power module 24 mounted to the major surface of the back plane 16 and electrically connected to the circuitry (column 32-38).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that a power module mounted to the major surface and electrically connected to the circuitry, as taught by Carlson because Carlson teaches such module provide power to service module (column 4, lines34-38)

Although, Jennison doesn't explicitly teach that major surface of the patch panel is the back major surface of the patch panel, it has been held In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that a power module mounted to the back major surface of the patch panel to provide power to service modules.

As to claims 7 and 13: Jannison discloses the patch panel having all of the claimed features as discussed above with respect claim 1(12),

except , Jennison doesn't explicitly teach a CPU module mounted to the major surface and electrically connected to the circuitry.

Carlson discloses in Fig. 1 control service module 22c mounted to the major surface of the motherboard 16 and electrically connected to the circuitry.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that a CPU module mounted to the major surface and electrically connected to the circuitry, as taught by Carlson because Carlson teaches such module can perform a variety of tasks (column 8, lines 49-57).

Although, Jennison doesn't explicitly teach that major surface of the patch panel is the back major surface of the patch panel, it has been held In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that a power module mounted to the back major surface of the patch panel to provide power to service modules.

5.3. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennison in view of Gerke, as applied to claim 1 above, and further in view of Curry et al. (Patent #6053764) hereinafter Curry.

As to claims 3 and 4: Jennison, as modified, discloses the patch panel having all of the claimed features as discussed above with respect claim 1, wherein one of the pairs of termination locations includes an RJ45 jack,

except , Jennison doesn't explicitly teach one of the pairs of termination locations includes two insulation displacement connectors.

Curry discloses in Fig. 1 one of the pairs of termination locations 18 includes insulation displacement connectors 19 (column 5, lines 22-27).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that one of the pairs of termination locations includes two insulation displacement connectors, as taught by Curry because Curry teaches such connections can be performed without adapters (column 4, lines 8-18).

5.4. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennison in view of Gerke and in view of Carlson, as applied to claim 8 above, and further in view of Curry.

As to claims 10 and 11: Jennison discloses the patch panel having all of the claimed features as discussed above with respect claim 8, wherein one of the pairs of termination locations includes an RJ45 jack,

except , Jennison doesn't explicitly teach one of the pairs of termination locations includes two insulation displacement connectors.

Curry discloses in Fig. 1 one of the pairs of termination locations 18 includes insulation displacement connectors 19 (column 5, lines 22-27).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Jennison to include in his invention that one of the pairs of termination locations includes two insulation displacement connectors, as taught by Curry because Curry teaches such connections can be performed without adapters (column 4, lines 8-18).

Relevant Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sajadi et al. – US Patent 6826280; Follingstad et al. – US Patent 6992257;
Wise – US Patent 7136290;

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571)- 272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

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1/19/07